ULTRA-HIGH ASPECT RATIO TRENCHES IN SINGLE CRYSTAL SILICON WITH EPITAXIAL GAP TUNING

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ABSTRACT

A new method for the formation of narrow (<100nm), smooth, ultra-high aspect ratio (>500:1) trenches in monocrystalline silicon is demonstrated using a combination of deep reactive ion etching (DRIE) and epitaxial deposition. Aspect ratios achieved were an order of magnitude higher than using DRIE only. This method was used to fabricate width-extensional mode resonators with narrow gaps within our wafer-scale epitaxial polysilicon encapsulation process. A representative 52 MHz width-extensional mode resonator with a motional impedance near 1 kΩ is carefully characterized.

KEYWORDS

High Aspect Ratio, Deep Reactive Ion Etching, Narrow Gaps, Silicon Trenches, Epitaxial Deposition, Resonators.

INTRODUCTION

The performance of capacitive MEMS devices depends strongly on the dimensions of the transduction region – narrow and deep trenches are often desired for maximum in-plane capacitive transduction. As such, a large importance is placed on the realization of such high aspect ratio trenches.

Deep reactive ion etching (DRIE), or the Bosch process [1], has become a key enabler for creating high aspect ratio structures in silicon and has been used extensively for MEMS, and more recently, dynamic random access memory (DRAM) capacitors and through-silicon-vias (TSVs). Repeatedly switching between reactive ion etching and passivation cycles, it is able to form features with vertical sidewalls. However, the switching results in scalloping of the sidewalls, which can be ameliorated by reducing the cycle times, but at the expense of etch rate. In addition, DRIE aspect ratios are usually limited to ~50:1, with ~100:1 achieved at best [2, 3], because of microloading and aspect ratio dependent transport effects [4]. Typical DRIE profiles exhibit a significant amount of taper inwards along the trench profile because of aspect ratio dependent transport effects, and are undesirable for most MEMS devices.

One way of achieving high aspect ratio trenches in silicon is to first etch a large feature into a single crystal silicon layer, then grow a sacrificial thermal oxide of the desired trench width, followed by a polysilicon deposition over the oxide. The release of the sacrificial oxide in HF then yields a narrow gap between polysilicon and single crystal silicon, e.g. the HARPSS process [5, 6]. However, for MEMS devices, this process also requires a secondary bonded cap to form a hermetic package, which increases size, adds cost, and necessitates a getter.

For high volume commercial applications, it is desired to leverage wafer-scale packaging techniques such as the epitaxial polysilicon encapsulation (*epi-seal)* process [7, 8] developed in our group and currently used at SiTime Corporation [9]. The *epi-seal* process provides a proven hermetic, ultra-clean environment for the stable operation of resonators, but transduction gap aspect ratios are limited to what is achievable with DRIE. Ideally, a hybrid HARPSS/*epi-seal* process would allow for high performance capacitive MEMS devices with exceptional stability [10, 11] in a low cost, high yield manufacturing process.

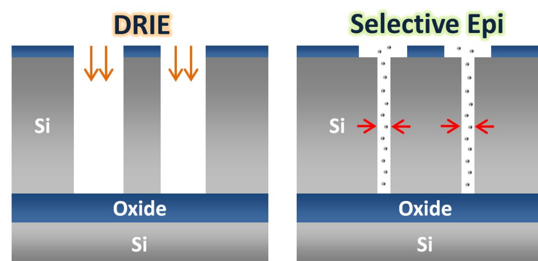


Figure 1: Process flow for forming ultra-high aspect ratio trenches on an SOI wafer.

However, the crucial step for the *epi-seal* process is the high temperature (> 1000°C) bake step in an epitaxial reactor prior to the seal – this bake step removes contaminants and native oxide to achieve the acclaimed stability. Polysilicon surfaces at these high temperatures are known to roughen due to silicon migration causing grain growth along the randomly oriented grains [12]. This roughening of polysilicon surfaces could cause the bridging of narrow transduction gaps, and this thus precludes the use of polysilicon in the *epi-seal* process. Single crystal silicon, on the other hand, have their crystalline surfaces *smoothed* during the bake step, removing DRIE scallops [13], and are hence advantageous for fabricating narrow transduction gaps in the *epi-seal* process.

To obtain high aspect ratio trenches with narrow gaps in single crystal silicon, an epitaxial gap tuning process [14] has been developed (Fig. 1). After an initial DRIE etch, scallops are annealed away in an epitaxial reactor and epitaxial silicon is deposited conformally on the sidewalls to reduce the gap. This combination of DRIE and epitaxial deposition can create sub-100nm width trenches between smooth, crystalline surfaces, while preserving the trench depth. Aspect ratios of >500:1 are thus demonstrated, with less than ±20% width variation along the trench profile. The addition of a single epitaxial process step is all that is necessary to tune the gap, and can be performed on bulk silicon as well as silicon-on-insulator (SOI) wafers for MEMS devices. A 52MHz width-extensional resonator with narrow gaps is demonstrated in this process.

FABRICATION

Ultra-high Aspect Ratio Trenches in Bulk Silicon

The fabrication of the narrow trenches begins with growing a 1.2 µm thermal oxide hard mask on a (100) 4” silicon wafer. Trenches with widths between 0.7µm to 1.5µm were patterned and etched into the hard mask. The silicon was then DRIE etched with a Multiplex Pro ASE HRM deep reactive ion etcher from Surface Technology Systems. Using a ramped recipe, aspect ratios of ~50:1 (trench depths of between 45 to 70 µm) were achieved with less than 20% width variation along the trench profile. The DRIE process alternates between SF_6 (etch) and C_4F_8 (deposition) chemistries, and the process parameters for the ramped recipe are listed in Table 1. A slight blow out is observed: 0.7 µm feature widths on the mask result in trenches that are about 1.0 µm wide along the trench depth, resulting from compounded lithography, hard mask etch, and DRIE processes. Different trench depths (Fig. 2) were observed for trenches of different widths due to aspect ratio dependent transport effects [4]. Around 0.8 µm of the hard mask was consumed during the DRIE process, with about 0.4 µm of oxide remaining.

Table 1. Process Parameters used for the DRIE (with linear ramping).

Process Parameter	Passivate (C_4F_8)		Etch (SF_6)	
Ramp	Start	End	Start	End
Cycle Time (s)	2.4	2	3	3
13.56 MHz Coil Power (W)	1200	1200	2000	2000
380 kHz Platen Power (W)	0	25	80	100
Pressure (mTorr)	18	18	9	9
C_4F_8 flow (sccm)	200	200	0	0
SF_6 flow (sccm)	0	0	200	200
O_2 flow (sccm)	0	0	20	20
Number of cycles	425 cycles (~37 min)			

Leaving the remaining oxide hard mask in place, the trenches were refilled using a selective epitaxial silicon deposition in and Applied Materials Centura Epi reactor. A selective recipe ensures that silicon is not deposited on oxide, but only on silicon surfaces. A high temperature bake step in the epitaxial reactor (1050°C for 3 minutes) prior to the deposition was performed to remove native oxide and also anneal out DRIE scallops. The selective epitaxial deposition was then done at 875°C at a pressure of 20 Torr with a H_2 carrier gas. Gas flow rates during the deposition were set at: 300 sccm SiH_2Cl_2 (dichlorosilane, DCS); 60 sccm 1% B_2H_6; 370 sccm HCl. The relatively low deposition temperature reduces the sticking coefficient, allowing for an extremely conformal deposition. This, however, also reduces the deposition rate ~20 nm/min (on each sidewall), but is not an issue since only ~400 nm of silicon is required to narrow the trench. The result is a deep trench (45 to 70 µm) that is extremely narrow (~80 nm) (Fig. 3), giving an aspect ratio of over 500:1, with single crystal silicon on both sides of the trench. This enables trenches with aspect ratios an order of magnitude higher compared to the DRIE-only solution.

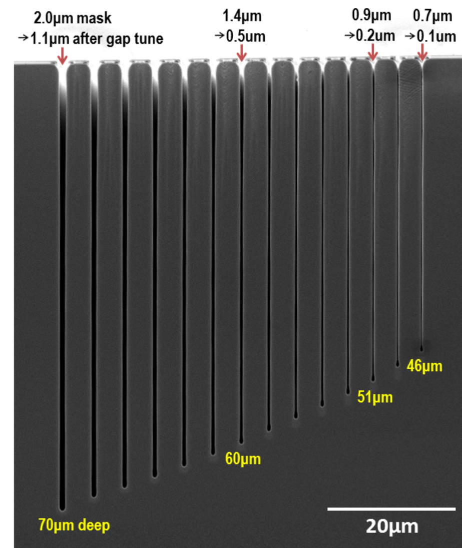
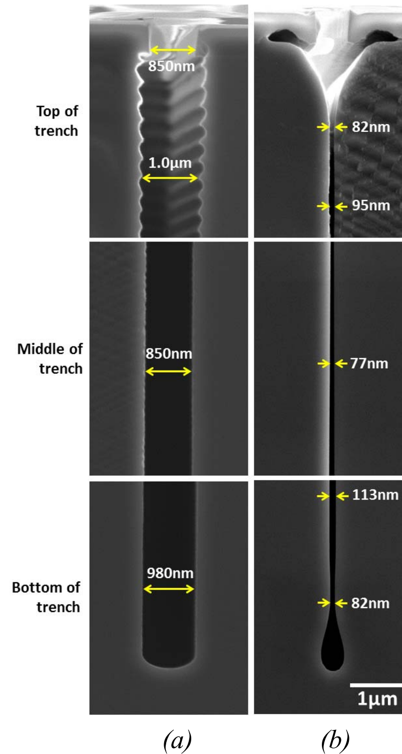


Figure 2: SEM of trench profiles of various gap sizes after DRIE and epitaxial gap tuning.



(a) (b)

Figure 3: SEMs of ~46µm-deep trenches in single crystal silicon using a 700nm mask. (a) Trench profile (top, middle, bottom) after DRIE etch. (b) Profile after epitaxial gap tuning.

Narrow Gap MEMS Resonators with *epi-seal*

For MEMS applications, trenches that define the movable structure can be patterned in the device layer of an SOI wafer, with the buried oxide under the movable structure acting as a sacrificial layer. Based on the results of the bulk wafer etching above, an SOI wafer with a 40 µm device layer was chosen to demonstrate the feasibility of epitaxial gap tuning for MEMS devices. Width-extensional silicon bulk acoustic resonators (SiBARs) similar to those in [6] were defined in this process. To enable the release of the resonator from the buried oxide,

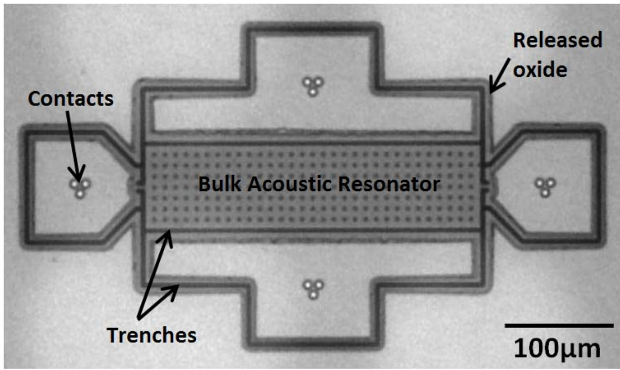


Figure 4: Infrared image of the silicon bulk acoustic resonator fabricated in the epi-seal process. The grey regions are the oxide-released areas.

etch holes/trenches were defined in resonator body (Fig. 4). Transduction trenches were defined with a 0.7 µm width on the mask, while electrical isolation trenches were defined with a 2.0 µm width. During the DRIE etch, the buried oxide acts as an effective etch stop, and notching at the base was minimized using a low frequency (380kHz) platen source. For the epitaxial gap tuning step, it is especially crucial for the deposition to be highly selective: deposition is only desired on the trench sidewalls; if silicon is deposited on the buried oxide, the trench can be bridged and hence prevent the release of the structure. Using a similar fabrication sequence as describe in the previous section, the transduction gap was narrowed down to ~250nm.

Resonators or other devices with narrow gaps defined by this method have single crystal silicon on both sides of the trench and are compatible with the *epi-seal* wafer-level fabrication process, and the encapsulation sequence can thus proceed. After the trenches have been defined, tetraethyl orthosilicate (TEOS) oxide is then used to define the spacer/isolation between the device and the encapsulation. The oxide seals over the narrow trenches, leaving keyholes that aid in the subsequent release etch – thick MEMS structures with narrow gaps can thus be released without requiring long etch times. After defining electrical contact holes in the oxide, an epitaxial polysilicon first cap is then deposited. Vents are defined in this cap and the oxide around the structure is then released with vapor HF. After a bake step in the epitaxial reactor, the device is sealed in the cavity by depositing epitaxial polysilicon over the vent holes. This provides a hermetic, ultra-clean, environment for the stable operation of resonators. Finally, electrical isolation and contacts are defined in the cap, completing the *epi-seal* process.

A caveat with the epitaxial gap refilling process is that the growth rate is dependent on the orientation of the crystal surface [15]. Thus, while tuning the width of trenches in one orientation, it is likely that trenches in other orientations may be over- or under-filled. Fig. 5 shows a top view optical micrograph of a ring-shaped trench that has uneven refilling. However, it may be possible to compensate for the different orientation growth rates in this process by defining trench widths appropriately in the mask layout.

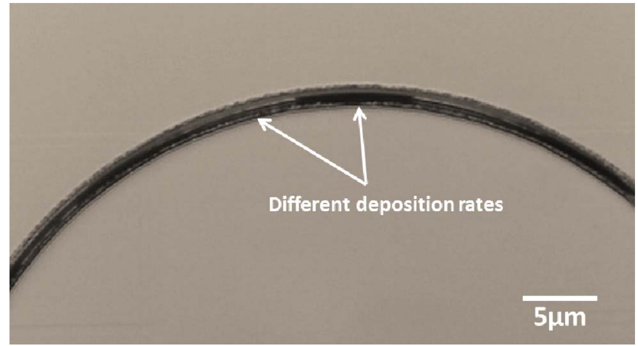


Figure 5: Uneven gap tuning of a circular trench as epitaxial deposition rates are crystal-orientation dependent.

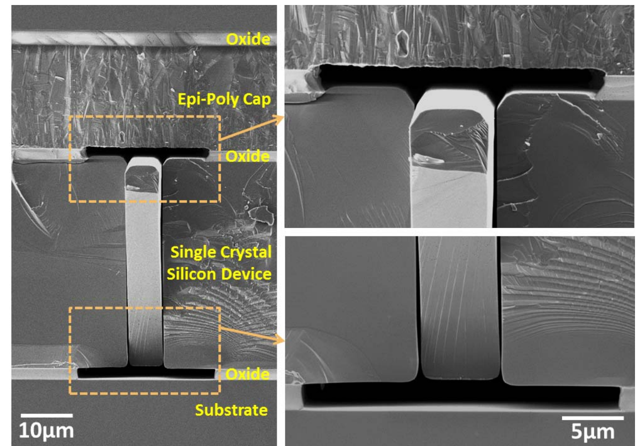


Figure 6: Cross-section SEMs of an encapsulated beam with ~250nm transduction gaps, exemplifying the structure of the resonators.

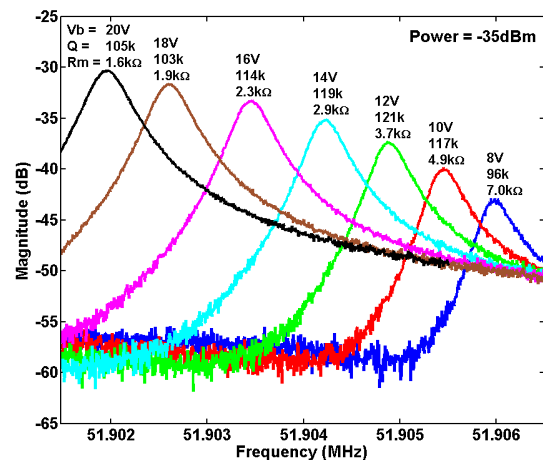


Figure 7: Frequency sweeps of the SiBAR resonator at different bias voltages, showing a resonant frequency at 51.9MHz with a quality factor of about 120,000.

RESULTS

The SiBAR resonator demonstrated in this process has dimensions 320 x 80 x 40 µm, corresponding to a width-extensional resonant frequency of 51.9 MHz. The

resonator was suspended on tethers that were 3 μm wide by 6 μm long. A released beam structure with narrow gaps exemplifying the cross-section of such resonators is shown in Fig. 6. Frequency sweeps reveal quality factors of 120k, consistent with similar devices that have been reported previously [6]. The dynamic response of the resonator as a function of bias voltage (Fig. 7) shows the reduced impedance as the bias is increased.

CONCLUSION

A fabrication method for smooth, narrow (<100 nm), ultra-high aspect ratio (>500:1) trenches in single crystal silicon is demonstrated using a combination of DRIE and epitaxial silicon deposition. The epitaxial deposition step smoothens and narrows the trenches, achieving aspect ratios an order of magnitude higher. Good control of the trench profile is achieved with less than ±20% width variation. Unlike polysilicon surfaces which roughen during an epitaxial high temperature bake, single crystal silicon surfaces are smoothed. This fabrication method enables narrow transduction gaps in an epitaxial polysilicon wafer-scale encapsulation process.

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REFERENCES

[1] F. Laermer, A. Schilp, "Method of anisotropically etching silicon", U. S. Patent 5501893, Mar 26, 1996.

[2] K. J. Owen, B. VanDerElzen, R. L. Peterson, K. Najafi, "High Aspect Ratio Deep Silicon Etching", in *Proc. MEMS*, pp. 251-254, 2012.

[3] F. Marty, L. Rousseau, B. Saadany, B. Mercier, O. Français, Y. Mita, T. Bourouin, "Advanced etching of silicon based on deep reactive ion etching for silicon high aspect ratio microstructures and three-dimensional micro- and nanostructures", *Microelectronics Journal*, vol. 36, pp. 637-377, 2005.

[4] J. Yeom, Y. Wu, J. C. Selby, M. A. Shannon, "Maximum achievable aspect ratio in deep reactive ion etching of silicon due to aspect ratio dependent transport and the microloading effect", *J. Vac. Sci. Technol. B*, vol. 23, pp. 2319-2328, 2005.

[5] F. Ayazi, K. Najafi, "High Aspect-Ratio Combined Poly and Single-Crystal Silicon (HARPSS) MEMS Technology", *J. Microelectromech. Sys.*, vol. 9, pp. 288 – 294, 2000.

[6] S. Pourkamali, G. K. Ho, and F. Ayazi, "Vertical capacitive SiBARs", in *Proc. MEMS*, pp. 211–214, 2005.

[7] A. Partridge, M. Lutz, "Episeal pressure sensor and method for making an episeal pressure sensor", U. S. Patent 6928879, Aug 16, 2005.

[8] R. N. Candler, M. A. Hopcroft, B. Kim, W.-T. Park, R. Melamud, M. Agarwal, G. Yama, A. Partridge, M. Lutz, and T. W. Kenny, "Long-Term and Accelerated Life Testing of a Novel Single-Wafer Vacuum Encapsulation for MEMS Resonators," *J. Microelectromech. Sys.*, vol. 15, pp. 1446-1456, 2006.

[9] SiTime Corporation. (2013). *Technology Overview*, Available: http://www.sitime.com/.

[10] B. Kim, R. N. Candler, M. Hopcroft, M. Agarwal, W.-T Park, and T. W. Kenny, "Frequency Stability of Encapsulated MEMS Resonator," *Sensors and Actuators A: Physical*, vol. 136, pp. 125-131, 2007.

[11] E. J. Ng, H. K. Lee, C. H. Ahn, R. Melamud, T. W. Kenny, "Stability of Silicon Microelectromechanical Systems Resonant Thermometers", *IEEE Sensors Journal*, vol. 13, pp. 987-993, 2013.

[12] E.J. Ng, S. Wang, D. Buchman, C.-F. Chiang, T.W. Kenny, H. Muenzel, M. Fuertsch, J. Marek, U.M. Gomez, G. Yama, and G. O'Brien, "Ultra-stable epitaxial polysilicon resonators," *Solid-State Sensors, Actuators, and Microsystems Workshop*, pp. 271-274, 2012.

[13] M.-C. M. Lee, M. C. Wu, "Thermal annealing in hydrogen for 3-D profile transformation on silicon-on-insulator and sidewall roughness reduction", J. Microelectromech. Sys., vol. 15, pp.338 – 343, 2006.

[14] A. Partridge, M. Lutz, "Gap tuning for surface micromachined structures in an epitaxial reactor", U. S. Patent 6808953, Oct 26, 2004.

[15] M. Bartek, P. T. J. Gennissen, P. J. French, P. M. Sarro, R. F. Wolffenbuttel, "Study of Selective and Non-Selective Deposition of Single and Polycrystalline Silicon Layers in an Epitaxial Reactor", in *Proc. Transducers*, pp. 1403 – 1406, 1997.

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