STABLE CHARGE-BIASED CAPACITIVE RESONATORS WITH ENCAPSULATED SWITCHES

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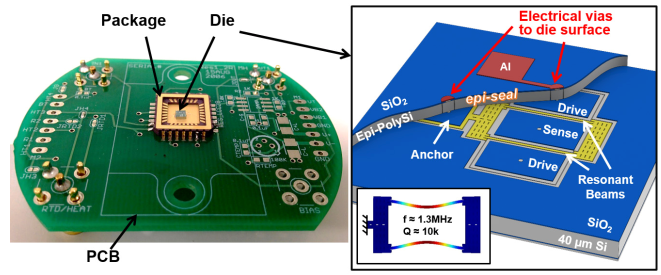
ABSTRACT

A large dc bias voltage (tens of volts) is often useful for the operation of capacitive MEMS devices. Charge-biasing techniques have been demonstrated to be able to replace a bias voltage source by trapping an equivalent charge on an electrically floating electrode. This work presents a charge-biased resonator that uses an electrostatically actuated mechanical switch with a pull-in voltage of 36 V to introduce a voltage-equivalent charge of 10 – 15V onto a resonant body. The switch and resonator are hermetically sealed in a clean vacuum cavity, within an epitaxial polysilicon encapsulation process (*epi-seal)*. No charge leakage has been observed, even at an elevated temperature of 125°C for weeks.

INTRODUCTION

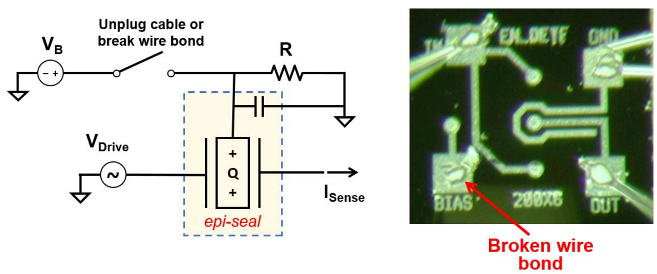
Many capacitively transduced MEMS devices are operated with a dc bias voltage to boost transduction. The bias voltage for typical resonators is usually in the range of tens of volts, and even higher voltages (hundreds of volts) are not uncommon, especially when large transduction gap sizes (> 1 µm) are involved [1]. To generate such high voltages in modern day CMOS requires charge pump circuitry and a substantial amount of power. The stability of the generated bias voltage is also of concern for ppb-stability MEMS resonators, as the frequency stability could be affected through the electrical softening effect.

Charge-biasing techniques have previously been demonstrated [2-5] and show great potential for low power timing references. By breaking off the electrical connection to a voltage-biased resonant body, a charge remains on the resonant body and performs the same function as a bias voltage. Once the charge has been applied, the bias voltage source is ideally no longer required, obviating the need for charge pumping circuits and hence conserving power. However, one caveat that has plagued the concept of charge biasing is that the charge can leak through parasitic resistances. As such, it is desired to increase the charge leakage time constant $\tau = RC$, and some demonstrated methods include: 1) increasing the stored charge by inserting a large capacitor [2]; 2) increasing the leakage resistance by controlling the environment, e.g. decreasing the temperature or humidity [6]; 3) trapping charge at the surface with an oxide-nitride layer [3, 5] or within an electrically floating electrode surrounded by oxide [4]. Of these methods, charge trapping is seen to work the most reliably, with 19 months of no observed charge leakage on an electrically floating electrode surrounded by a thick 3 µm layer of oxide for a capacitive micro-machined ultrasonic transducer in [4].



(a) *(b)*

Figure 1. (a) Printed circuit board with a gold package and an epi-sealed resonator die. (b) Cutaway schematic of an epi-seal encapsulated DETF resonator.



(a) *(b)*

Figure 2. (a) Circuit schematic for charge-biasing the resonator. The bias voltage supply is disconnected from the resonator, leaving a charge on the resonant body. The charge can then leak out through parasitic resistances. (b) A broken bias voltage wire bond to the die.

With the *epi-seal* encapsulation process demonstrating excellent long term stability for resonators [7], it is desired to investigate if the stability of such charge-biasing techniques extend to *epi-seal*ed devices with silicon surfaces free of native oxide and similarly anchored on a thick buried oxide layer.

CHARGE LEAKAGE

To investigate charge leakage from the resonant body, initial experiments were performed involving two different methods of electrically isolating the resonant body. A well-characterized double-ended tuning fork (DETF) resonator [8] fabricated within the *epi-seal* process was first mounted on a gold package, which was then soldered to a printed circuit board (PCB) as shown in Fig. 1. Frequency sweeps were performed on the device using an Agilent 8753ES network analyzer. A bias voltage was applied to the resonant body, and thereafter disconnected abruptly to leave

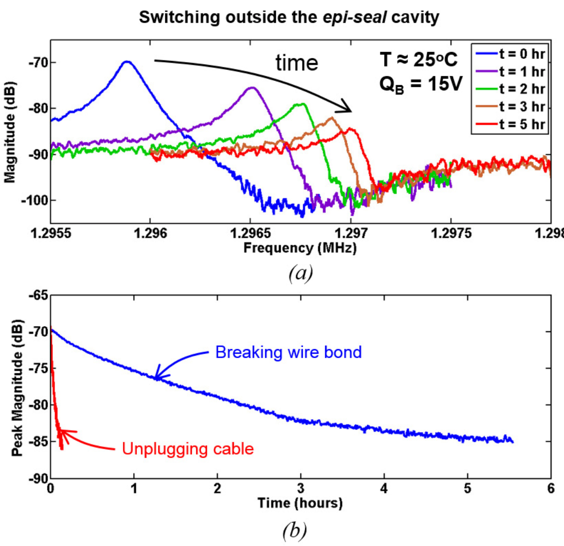


Figure 3. (a) Resonant peak decay when charge-biased by breaking the bias voltage wire bond to the die. (b) The transient peak decay after breaking the wire bond and unplugging the cable from the PCB.

a charge on the resonator. The circuit diagram is shown in Fig. 2a and the bias voltage can be disconnected by either unplugging the bias voltage cable to the PCB, or by breaking the wire bond (Fig. 2b).

Measured results at room conditions show that charge leakage ensues once the bias voltage is disconnected, as observable from the resonant peak decay (Fig. 3a). Plotting the transient peak magnitudes (Fig. 3b), a much faster leakage is noted for the case of unplugging the bias voltage cable, compared to breaking the wire bond directly off the die. This could be due to parasitic leakage paths present on the PCB, package, and connectors. To achieve stable resonators, the question then becomes: Can the parasitic resistances be removed almost entirely such that no noticeable leakage occurs?

*EPI-SEAL*ED CHARGES

Flash memory today is an example of extreme charge retention. Fowler-Nordheim tunneling is used to introduce tens of electrons onto a floating gate electrode sandwiched between dielectric layers, and these electrons are reliably trapped for years.

For reliable charge-biasing of capacitive MEMS devices, there similarly needs to be: 1) an environment through which charges cannot dissipate, and 2) a method for introducing charges with zero leakage through the charge-introduction mechanism. It is noted that long term charge trapping is achieved in [4] by having the electrically floating electrode entirely covered with a thick oxide (3 µm) and using an extremely high electric field (a few MV/cm) to inject charge into the floating electrode.

In this work, a similar approach is taken, but instead of having the electrically floating electrode entirely covered with a thick oxide layer, only the resonator anchor sits on the thick buried oxide layer; elsewhere, the silicon surfaces

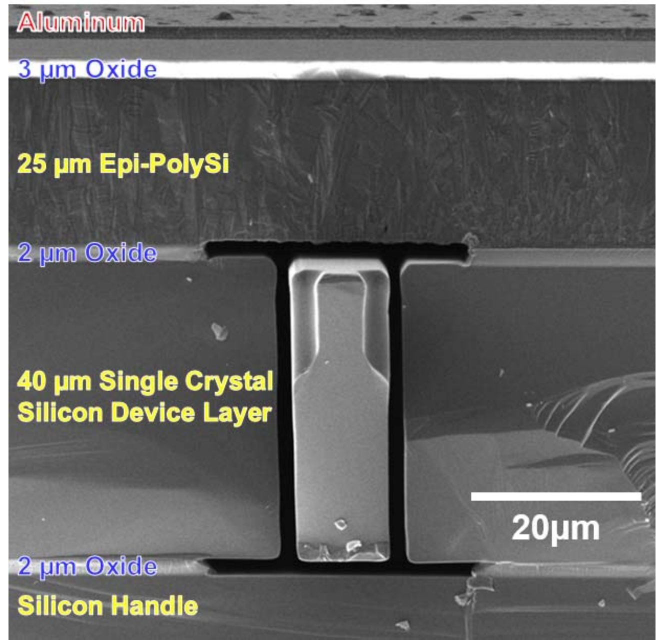


Figure 4. Cross-section SEM of an epi-seal encapsulated representative beam.

are free of native oxide and within the *epi-seal* cavity, which provides the closest-to-ideal packaging environment for MEMS demonstrated thus far, with a clean, hermetic vacuum encapsulation [9]. Charges are then introduced with a mechanical contact switch located within the *epi-seal*ed cavity to reduce the charge leakage pathways. This has the added benefit of leveraging the existing *epi-seal* fabrication process without any modifications – in other words, these switches can be included for free.

Fabrication Process

The e*pi-seal* process is a high vacuum (sub-Pa), ultra-clean (high temperature seal, native oxide-free), high yield, wafer-scale commercial process. For this fabrication run, a 40 µm-thick, n-doped (antimony doped, ~1e18 cm^{-3}) device layer was used. The cross-section of a beam representing the final encapsulated resonating and switching beams is shown in Fig. 4. The device is surrounded by inert gas in the hermetically *epi-seal* cavity, and the electrically floating anchor of the resonant body sits only on the buried (lower) silicon oxide layer, which at 2 µm-thick is a near-ideal electrical insulator.

Electrical Isolation by Switching within *epi-seal* Cavity

A mechanical contact switch can be realized by means of a clamped-clamped beam amongst many possibilities. In this work, a 300 µm long by 3 µm wide clamped-clamped beam was designed to be electrostatically pulled towards a pair of gate electrodes (Fig. 5a). The gap varies linearly from 0.7 µm at the end to 1.5 µm at the middle (Fig. 5b), designed to help reduce the pull-in voltage but also to prevent collapse of the beam into the gate. At the center, a 6 µm wide contact post, which is connected to the resonant

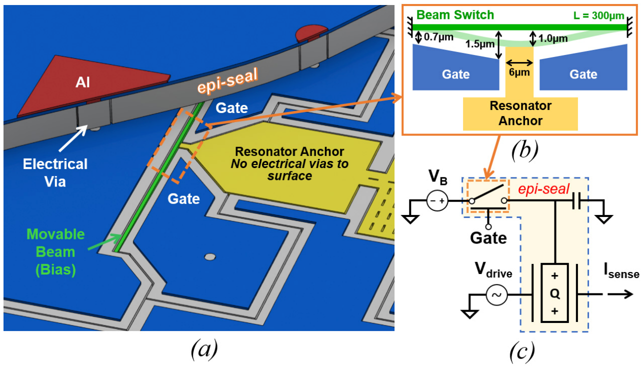


Figure 5. (a) Design of contact switch within the epi-seal cavity. (b) The beam can be pulled in to make contact with the resonator anchor for charge introduction. (c) The switch is now placed within the epi-seal cavity, compared to Fig. 2.

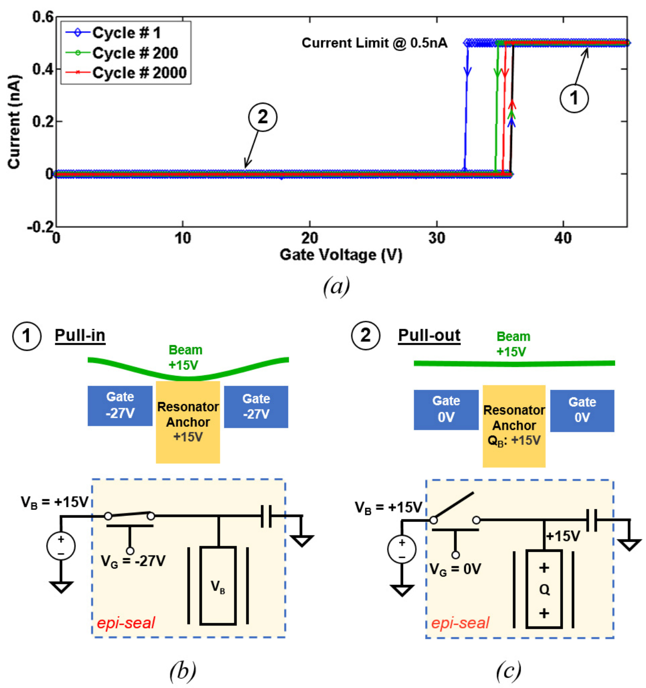


Figure 6. (a) Measured pull-in / pull-out characteristics of a mechanical beam switch. (b) The desired voltage is applied to the beam and the remaining voltage difference required for pull-in is applied to the gate. (c) The gate voltage is then zeroed, allowing the beam to pull out. The bias and gate voltages can subsequently be released.

body's anchor, protrudes out by 0.5 μm to physically contact the center of the pulled in beam and prevent the beam from collapsing into the gate. The circuit diagram is shown in Fig 5c, and it is worth emphasizing that the switch is placed within the *epi-seal* cavity. The resonant body's anchor, unlike that in the previous test (Fig. 1), has no electrical via and is hence isolated from the die surface. Charges are introduced to the resonant body when the beam is pulled in, and once the beam has pulled out, there is effectively no electrical pathway for leakage.

In an effort to first experimentally characterize the pull-

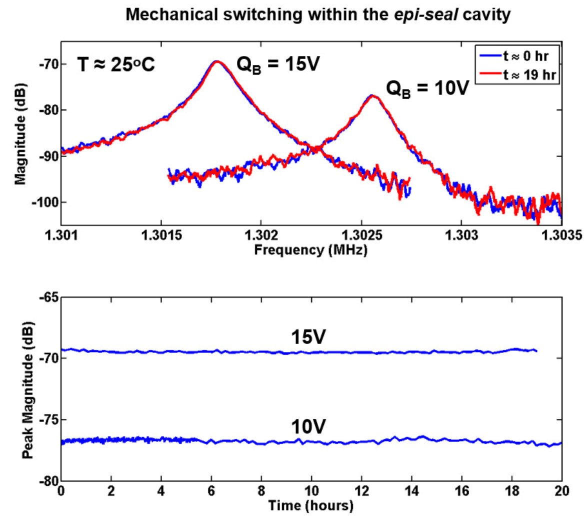


Figure 7. Voltage-equivalent charges can be applied with no noticeable leakage. The charge can be reprogrammed by repeating the same pull-in / pull-out technique.

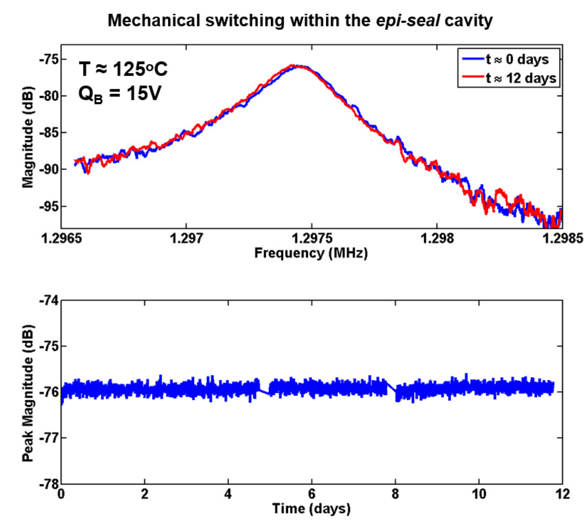


Figure 8. No charge leakage was observed, even at elevated temperatures of 125°C.

in switch mechanism to the isolated resonant body's anchor, an identical switch mechanism was designed, but this time with an electrical connection to the contact post such that the beam contact can be sensed via a resistance change between the beam and the contact post. Pull-in and pull-out characteristics are seen (Fig. 6a), with the current limit set to 0.5 nA for this characterization to prevent burning out the switch. The pull-in voltage is seen to be about 36 V and the pull-out voltage ranges from 32 to 35 V. It is also seen that thousands of pull-in/pull-out cycles can be performed, allowing for the introduced charge to be reprogrammed multiple times.

When charging an actual resonator, it is difficult to detect pull-in as no electrical vias are present on the resonant body's anchor. Thus, it is assumed that the pull-in voltage remains within the same range as the characterized beam, and to be certain that the beam is pulled in, a slightly higher voltage difference (in this case 42 V, compared to the measured 36 V) is assumed to be required for pull-in. The desired voltage for the resonator (e.g. +15V) is applied to the beam, and the remaining voltage difference for pull-in (e.g. -27 V) is applied to the gate (Fig. 6b). The surrounding field potential is held at ground.

Reducing the gate voltage to ground (Fig. 6c) then causes the beam to pull-out, breaking the electrical contact with the resonant body while biased at the desired voltage (e.g. +15V). The applied voltages on the beam and gate can then be removed. The electrically floating resonant body is now anchored on the buried oxide layer and is entirely within the *epi-seal* cavity with no electrical connection to the outside of the cavity.

Fig. 7 shows the frequency sweeps of a resonator that has been charged with bias voltages of 10 V then reprogrammed to 15 V, with a difference in the peak magnitude as expected. No leakage is noticed even after 19 hours at room conditions. To further confirm the stability, the device was heated to 125°C and held for 12 days – again no charge leakage was noticed (Fig. 8), attesting to the inert environment of the *epi-seal* cavity.

CONCLUSION

Demonstrated in this work is a resonator that is charge-biased by mechanical contact switching within an *epi-seal* cavity – a well-controlled inert environment. A voltage-equivalent charge can be programmed multiple times as desired with no charge loss detected, even at an elevated temperature of 125°C. This may obviate the need for circuitry to maintain a stable dc bias voltage and reduce the required power for capacitive MEMS resonators. Further long-term stability testing is underway, but the experimental confirmation thus far of the absence of charge leakage pathways also provides further evidence for the ultra-clean nature of the *epi-seal* environment.

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