Wafer Scale Encapsulation of Wide Gaps using oxidation of Sacrificial Beams

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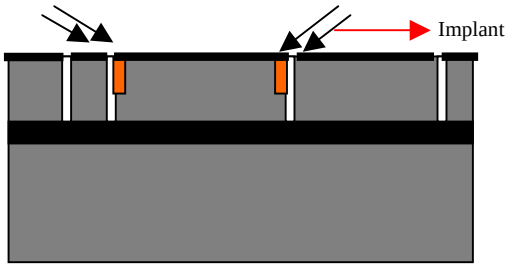
Abstract—This paper explores the possibility of using oxidation of sacrificial beams to encapsulate wide gaps. This method of oxidizing silicon beams in order to create diffusion barriers and structural supports has been reported in literatures. The idea is to encapsulate gaps of various widths in a method that is independent of the width of the gaps. In this experiment we try to encapsulate devices and structures with large gaps of the order of 10-20 μm using this technique and observe the results through SEM images.

1. Introduction

Traditionally MEMS devices are packaged using various wafer bonding techniques [1,2]. This unfortunately has the drawback that it requires a seal ring, which consumes a lot of die area. Wafer bonding technique also increases the area required on the die, as bond pads cannot be placed directly over the device cap. The process of wafer scale encapsulation helps in overcoming these problems and miniaturizing the size of MEMS devices. The encapsulation eliminates the need for cap wafers and any alignment problems due to misalignment of the device wafer with the cap wafer.

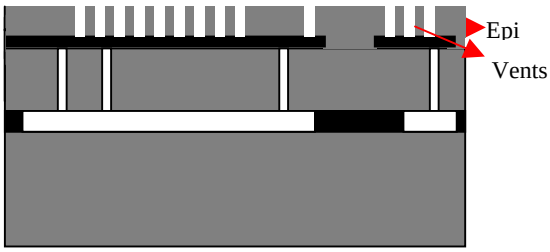
Bosch (RTC) and Stanford University have developed a wafer scale encapsulation process that can be used to seal devices like accelerometers and high frequency resonators. This process called “oxide-seal” involves DRIE etching the device pattern into device layer of a SOI wafer and then implanting required areas of the wafer with boron dopants to form the piezoresistors. The trench or gap width for the devices is usually restricted to 1.5-2.0μm. The process of doping for accelerometers usually involves top implant and side implants. The side implants are usually done after covering the areas that do not require implants with oxide or resist. The gaps and device structures are sealed with a sacrificial material such as silicon dioxide [3,4]. This also forms the structural support over which the encapsulation layer is deposited after patterning. Silicon dioxide is chosen because of the ease of depositing LPCVD oxide and the fact that HF can remove it easily in liquid or vapor form [5,6]. A thick encapsulating layer of P-doped silicon is grown on top of the patterned silicon dioxide using a non-selective Epitaxial silicon deposition. The non-selectivity is important in order to obtain a conformal coating of silicon over the entire wafer. The wafers are then polished using CMP to obtain a flat surface. The wafers are then patterned and etched to form vents that are used to introduce HF vapor to remove the sacrificial oxide and release the device. The vents are etched all the way down till the deposited oxide layer. This also helps in isolating the electrical contacts. The vents are then sealed using LTO silicon dioxide deposition [3,4]. The oxide is then patterned and etched to create electrical contacts. Finally a thin layer of aluminum is deposited and patterned to form interconnects. This allows vertical interconnects that again saves die space. Fig 1 shows the various steps involved in encapsulation process.

a) DRIE etching of pattern into device layer

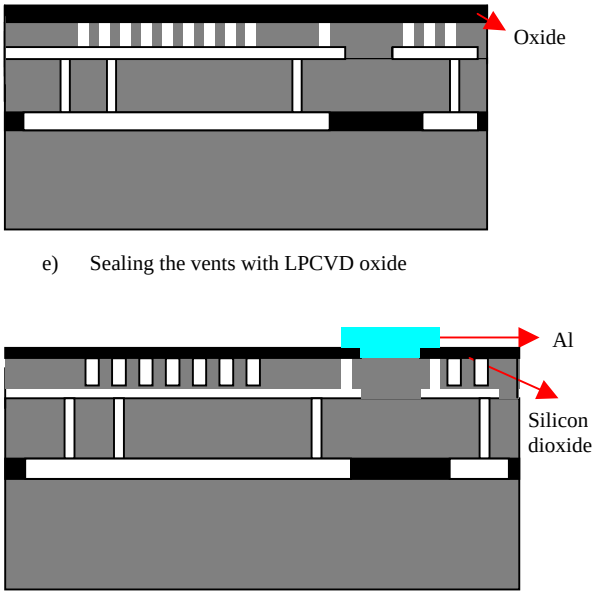


b) Implant to form piezoresistor

c) LPCVD oxide to seal the gaps and device



d) Encapsulating silicon deposition and vent etch



e) Sealing the vents with LPCVD oxide

f) Al interconnects sputtered after patterning oxide

Fig1. Device Fabrication using oxide-seal

2. Device Characterizing

By utilizing the process described, the encapsulated accelerometers were successively fabricated and characterized. [4] The characterization and performance of the accelerometer are discussed below:

2.1 Frequency Response

The frequency response of some devices fabricated by the process described above. The frequency response is measured by shaking the accelerometer with a piezoelectric vibration exciter. The acceleration is measured using a laser Doppler vibrometer. A vector signal analyzer collects the vibrometer signal and accelerometer response to calibrate the frequency response. With the frequency spectra, we can easily determine the Quality Factor of the device by the following equation:

$$Q = \frac{Amp_{resonant}}{\Delta Freq_{\pm 3dB}} \qquad (1)$$

Quality factor plays an important role in high-sensitivity accelerometer because it will determine the thermomechanical noise of the device. [7]

$$A_{Thermal} = \sqrt{\frac{4k_B T_{room}\omega_0}{m_p Q}}\ [g/\sqrt{Hz}] \qquad (2)$$

For high-sensitivity accelerometer, the minimum detectable acceleration will be constrained by both thermomechanical and electrical noise. Hence increasing the quality factor of the device can help reduce the mechanical noise and achieve better resolution.

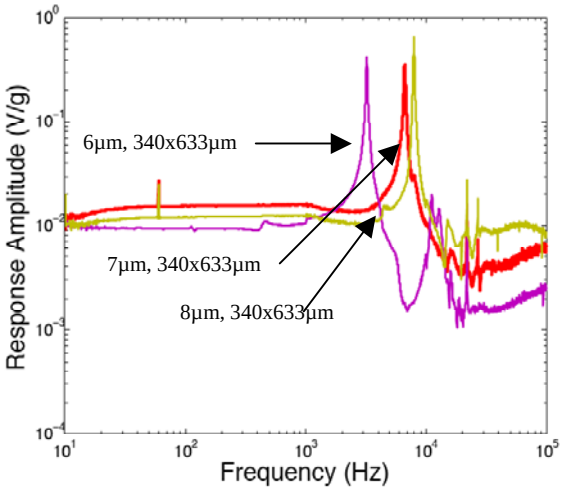


Fig 2. Frequency response of accelerometers with proof mass size and flexure width

2.2 Noise Density

The noise density spectrum of two typical encapsulated devices is shown in Fig. 3. Previous work has shown that this encapsulation technique improves the noise density in both 1/f and Johnson noise region. Furthermore, it also shows that the noise density becomes comparable to the theoretical value of the resistive device. [4]

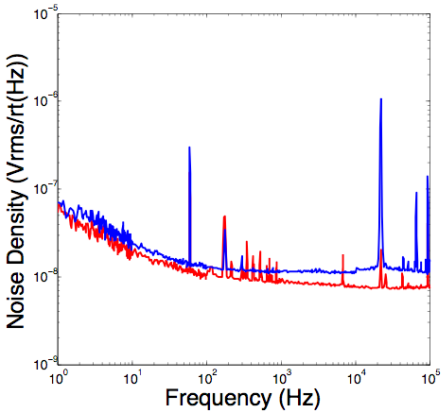


Fig 3. Noise density spectrum of two typical devices. The difference of the noise floor is due to different resistances of the devices.

From the frequency response and noise density spectra, the resolutions of the devices were found to fall into the sub-milli g region.

2.3 Dynamic Range

The dynamic range of the accelerometer is restricted by the width of the gap between proof mass and the proximal sidewalls. Due to the restriction of the previous process, a 1.5µm gap limits the movement of proof mass

while it is experiencing intense acceleration. Therefore, large gap between the proof mass and sidewalls is favorable to achieve a higher dynamic range.

The miniature accelerometer developed in our group has been packaged and applied in various biomedical projects, including fully implantable sensor of cochlear implants, heart rate sensor for neonatal mice, optical insertion sensor for traumatic optic neuropathy studies and motion tracking sensor for endoscope applications. [8]. The results demonstrate very promising outcomes in biomedical applications. However, some of the preliminary results also show the needs for higher sensitivity and higher dynamic range accelerometer, which are some of the motivations for developing this new encapsulation process.

2.4 Performance Enhancement

In order to have better resolution and range we need to improve on two things

1) Increase the Quality Factor: This can be achieved by having a lower vacuum inside the encapsulation.

2) Increase the gap width between the device and sidewalls in order to increase the range.

The Quality factor depends on the pressure inside the encapsulated chamber. In order to reduce the pressure inside the chamber we need to be able to drive out the residual gases present inside. This can be done using nitrogen annealing at 400^0C. In order to implement this the fabrication process is slightly modified and devices are sealed using an alternate wafer scale encapsulation process which involves sealing the devices during the epitaxial silicon deposition. [9]. It has already been proven in previous works that sealing a device with silicon or polysilicon helps in reducing the pressure inside the encapsulation due to easy removal of the residual hydrogen gas. [10]. The problem of encapsulating a wide gap is slightly more complicated and will be dealt with in the next section.

4. Encapsulation of wide gaps

The LPCVD oxide deposition is a critical step in the wafer scale encapsulation process. It not only seals the gaps and trenches of the devices but also forms the structural support over which the encapsulating layer of Epitaxial doped silicon is grown. At a later step this oxide is removed and the device gets released, leaving behind the device and a large gap encapsulated by epitaxial silicon and the SOI wafer handle wafer. The LPCVD oxide is deposited using LTO in a furnace at 400^0C in the Stanford SNF Facility. The deposition rate of the oxide varies with temperature and the spacing between two wafers. It is observed that if the wafers are not too close and are evenly spaced the furnace achieves a deposition rate of 1μm per hour with less that 4% non-uniformity. This process relies on preferential deposition of silicon dioxide on the sidewalls due to shadowing effect for sealing of the gaps. The gaps in this process are not completely re-filled with oxide but oxide gets deposited preferentially at the top edge of the sidewalls, which seal the device within the sacrificial oxide. A set of LTO depositions were carried out on gaps of various widths to determine the thickness of oxide required for sealing the gaps. It is observed that the thickness of the LTO oxide required to just seal a gap is the same as the width of the gap. This means that wider the gap more oxide would have to be deposited in order to seal it. In order to have a safety margin a film thickness 1.5 times the gap width that has to be sealed is deposited. This is illustrated in Fig 4a and b.

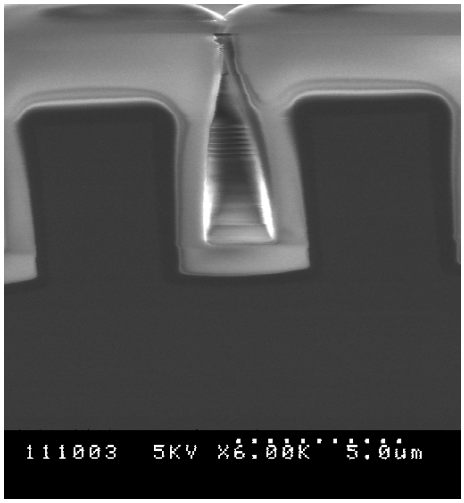


Figure 4a. A 5μm wide gap just sealed by 5μm thick oxide.

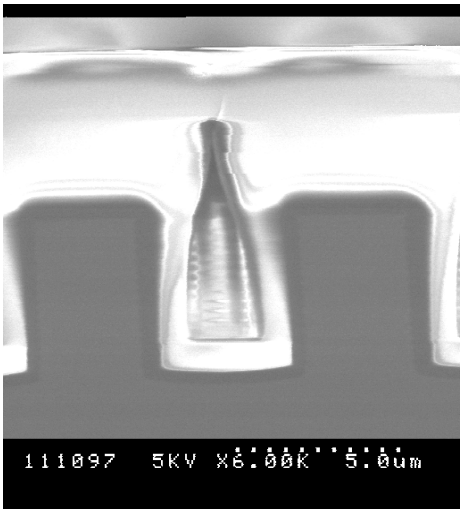


Figure 4b. A 5μm wide gap sealed by 7μm thick oxide.

4.1 Disadvantages

The sealing of the gaps is critical in order to have a platform on which the encapsulating layer of epipoly can be deposited. If the gaps were not completely sealed the silicon would get deposited in the gaps. Since it is impossible to remove this deposited silicon at a later stage, it would obstruct the movement of the device and thus affect its performance. Sealing narrow gaps would

be easy with this method but the only way to encapsulate wide gaps using LTO deposition would be to deposit a very thick film of oxide. The disadvantages of this method are

1) The time taken to deposit thick oxide would be very large. To seal a 10μm wide gap would take in excess of 12 hours.

2) The thickness of oxide film needed to seal all the gaps would depend on the largest gap width and even smaller gaps would have a very thick layer of oxide on top.

4.2 Oxidation of sacrificial beams

These above mentioned problems could be overcome if instead of depositing oxide on top of the wafer, we could somehow preferentially fill the gaps with oxide. Oxidation techniques have been used before to create structural supports and diffusion barriers [11,12]. These make use of the property of volume expansion of silicon on being oxidized. The process of selecting the right width of the sacrificial beam has been described in earlier works [13]. This oxidation technique achieves the following purposes:

1) Complete oxidation of beam results in volume and hence expansion of the sacrificial beams width. This results in a preferential oxide growth along the width of the gap.

2) The large reduction in the gap helps us seal them up with a very thin layer of LTO oxide.

3) The time to seal any gap depends on the width of the sacrificial beam alone.

It was determined through earlier work that a sacrificial beam width of 2.2μm spaced 1.5μm apart are completely oxidized after 7 hrs and 35 mins of wet oxidation at 1100^0C are completely oxidized. Depositing another thin layer of LTO oxide and a small etch-back results in complete sealing of the wide gap and formation of a smooth platform for depositing encapsulating silicon. This is shown in Fig 5.

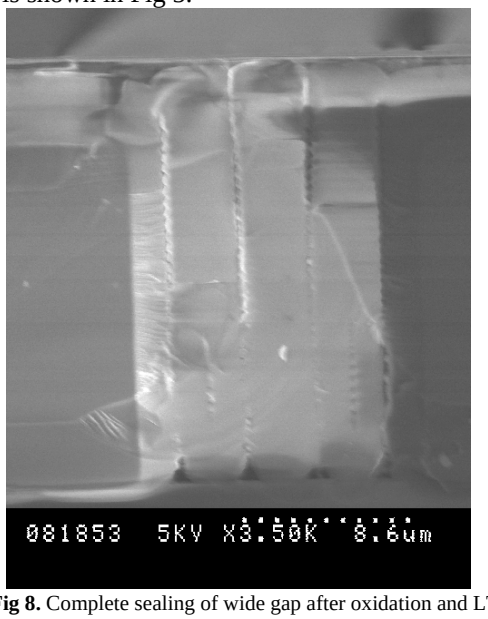
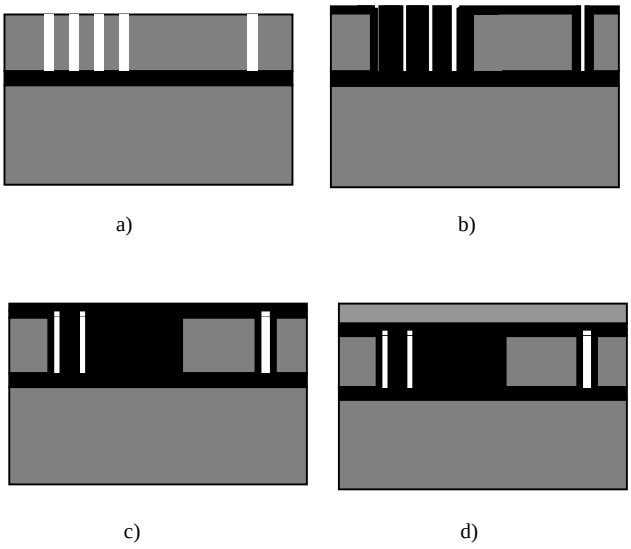


Fig 8. Complete sealing of wide gap after oxidation and LTO deposition

5. Fabrication

Having obtained the optimum sacrificial beam width and the time for complete oxidation of these beams. We have incorporated these design changes into a standard wafer scale encapsulation technique developed in our group earlier [3,4,9]. The pattern of the device is etched into the SOI wafer using standard lithography and DRIE etching techniques. In addition to the device pattern sacrificial beams are also etched into the SOI, where wide gaps are required as shown in Fig 9a. The next step is wet oxidation, which is carried out in a furnace at 1100^0C. It is necessary to ensure that all the supporting material is oxidized to silicon dioxide. This is necessary to ensure that after the release of the devices there is no un-oxidized silicon debris left inside the cavities. During oxidation the beams expand in volume and fill out the gaps between them as shown in Fig 9b. This reduces the thickness of LTO oxide that needs to be deposited in order to seal the gaps. Once all the trenches are sealed using LTO we pattern the oxide and remove oxide from areas around the device. This leaves behind the device completely covered and buried in oxide while the rest of the wafer has silicon exposed. We then deposit 3μm of Epitaxial silicon at 950^0C on the wafer using a non-selective P-doped epitaxial deposition that coats the wafer surface in a conformal manner as shown in Fig 9d. The non-selectivity is obtained by initially seeding the oxide with SiH_4. The wafer is then patterned and etched to create vents on the wafer which are used for HF vapor etch. This removes the sacrificial beams and oxide from the device layer and releases the device by removing the buried oxide underneath as shown in Fig 9f. After the release a second round of selective P-doped epitaxial silicon deposition seals the wafers completely as in Fig 9g.



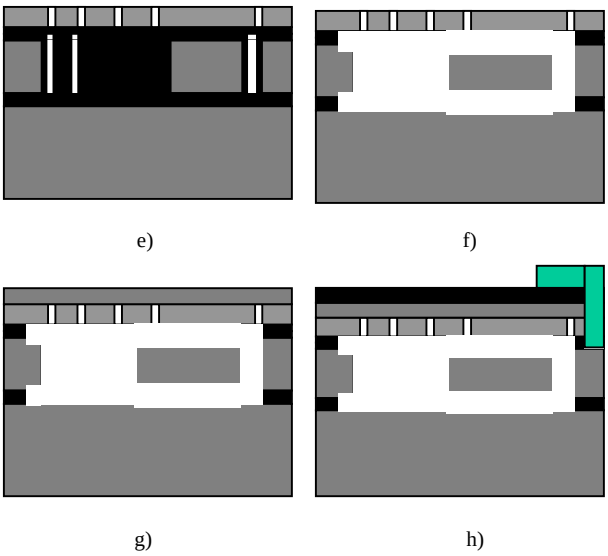


Fig 9. Main steps in the process for encapsulating wide gaps.

This epi-poly deposition of silicon leads to sealing of the device inside the newly formed cavity. The epi-poly seals the device at 10 torr at 950^0C. In case a high vacuum is required the device can finally be annealed in nitrogen ambient to drive out the residual hydrogen gas . Pressures as low as 1 Pa have been reported using the above mentioned "epi-seal process" [9]. About 30μm of silicon is deposited and then the surface is polished using CMP to obtain a flat surface on top. This is also important in order to continue further surface processing. The next step is to isolate the electrical contacts from the cap poly by DRIE etching of contact isolation rings, which are etched all the way into the cap poly till the device layer. This step is added because the vents are etched and resealed earlier as compared to the oxide-seal technique described earlier. This isolation ring is then sealed using another LTO deposition. Aluminum is then sputtered on the wafer and patterned to create interconnects.

6. Results

A characterizing run was carried out using this modified epi-seal process in order to ascertain the feasibility of encapsulating devices with very large gaps. One important result that needs to be kept in mind while designing is that during oxidation device structure also lose silicon and hence devices where resonant frequency is of importance must be compensated for changes in the beam width. If the devices are driven laterally into resonance then it is sufficient to compensate the width of the resonating structure, as the thickness does not affect the resonant frequency. Two important results were verified using this fabrication run,

1) Complete oxidation of 2.2 μm wide sacrificial beams is done by wet oxidation at 1100^0C by oxidizing for 7 hrs and 35 mins.
2) The wide gap is completely sealed after deposition of a thin layer (1-2μm) of LTO oxide.

The loss of device width due to oxidation is the twice the amount of silicon lost from the top surface. It is observed that after oxidizing for 7hours and 35 minutes about 0.85-0.9μm of silicon is lost from the top of the wafer while about 1.8μm from the sides. The loss of almost twice the thickness of oxide from the sides of the beams as compared to the top of the wafer is due to the fact that silicon beams are exposed to oxidation from both the sides as opposed to silicon on top, which only gets oxidized from one side. On the whole it is important to remember while designing structures that lateral width would be compromised by about 0.5μm due to DRIE etch and 1.8μm due to oxidation. Hence it is necessary to design structures with a compensation margin of 2.3 μm to ensure than finally the devices have the required width.

The results of these characterizing experiments have shown that it is possible to build a wide SiO_2 structure in the middle of our encapsulated device. Once the trench gaps have been significantly reduced, we proceed as discussed in the fabrication section. HF vapor etch was carried out for about 150 mins to release the devices. The HF vapor being gaseous does not stick to the surface and hence the problem of stiction does not arise. The progress of the HF vapor etch front is monitored using IR microscope to ensure that all the devices are completely released. The released structures after encapsulation are observed to have large encapsulated trenches of the order of 10-20μm. Fig 10-12) shows some of the encapsulated structures along with the large gaps.

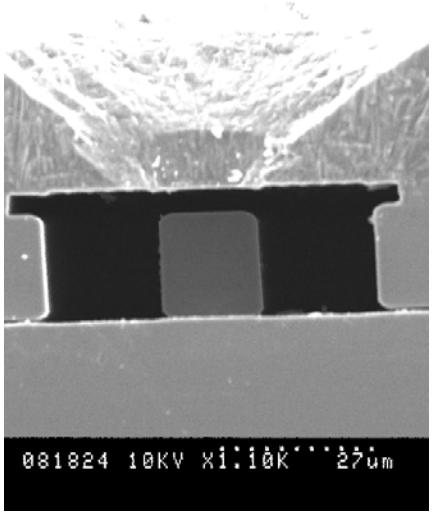


Fig 10. A completely releases flexure with 20μm wide gaps.

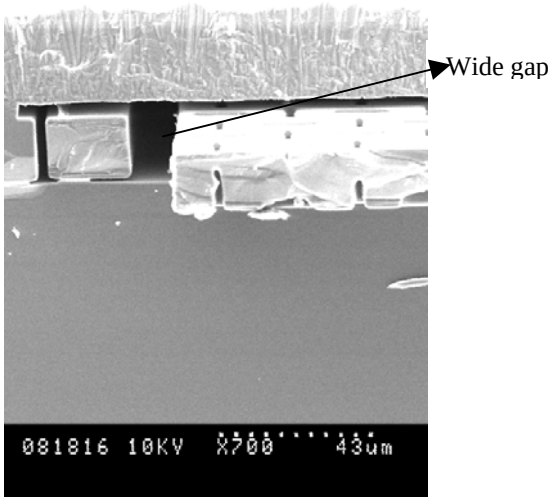


Fig 11. Encapsulated proof mass with a wide gap for larger range.

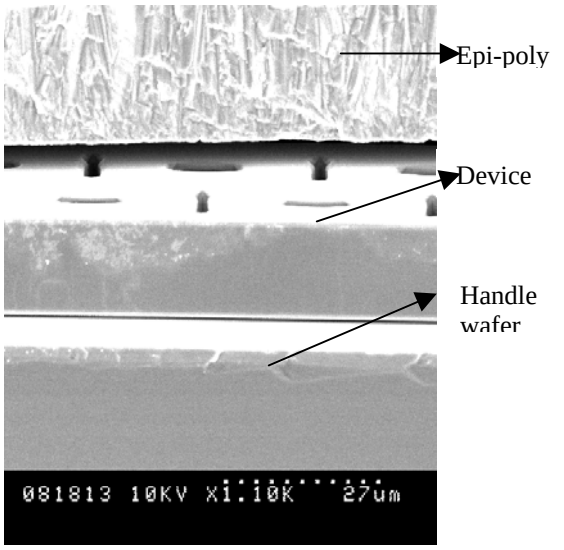


Fig 12. A cross section of the device showing various layers

7. CONCLUSIONS AND FUTURE WORK

The main achievement of this work is to demonstrate the feasibility of using oxidation of sacrificial beams as a tool to overcome the difficulties in encapsulating wide gaps. Using this technique we have encapsulate various structures with large displacements on a wafer scale. In future we would like to successfully demonstrate a working inertial sensor, which has been designed and fabricated in concurrence to this method. The same approach is applicable to other recently published film encapsulation processes [14-16].

ACKNOWLEDGEMENT

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